CLAIMS

What is claimed is:

1. A wafer test method, comprising the steps of:

providing a wafer integrally formed of a plurality of chips, each of the chips having an active surface and an opposite inactive surface, with a plurality of bond pads formed on the active surface;

preparing a conductive interposer having a first surface and an opposite second surface, wherein the first surface is formed with a plurality of test pads, and the second surface is formed with a plurality of test bumps electrically connected to the test pads, the test bumps corresponding to the bond pads of the chips, and mounting the conductive interposer on the wafer such that the test bumps are in electrical contact with the bond pads to electrically connect the conductive interposer to the chips; and

using test probes to contact the test pads of the conductive interposer to perform tests for the chips of the wafer.

2. The wafer test method of claim 1, wherein the conductive interposer is composed of a plurality of interposer units each corresponding to one of the chips.
3. The wafer test method of claim 1, wherein edges of the conductive interposer are supported by a frame that abuts against the wafer to position the conductive interposer on the wafer.
4. The wafer test method of claim 1, wherein the conductive interposer comprises a core having the first surface and the second surface, a plurality of conductive traces formed on the first surface and the second surface of the core, and a plurality of conductive vias penetrating the core for electrically connecting the conductive traces on the first and second surfaces of the core.
5. The wafer test method of claim 4, wherein the core is a thin film.

6. The wafer test method of claim 4, wherein the core is a substrate made of an organic material.
7. The wafer test method of claim 6, wherein the organic material is selected from the group consisting of epoxy resin, polyimide resin, BT (bismaleimide triazine) resin, and FR4 resin.
8. The wafer test method of claim 4, wherein the conductive traces are made of copper.
9. The wafer test method of claim 4, wherein the conductive vias are formed by plating copper in a plurality of through holes penetrating the core.
10. The wafer test method of claim 4, wherein a solder mask is applied over the first surface of the core and formed with a plurality of openings for exposing predetermined portions of the conductive traces, and the exposed portions serve as the test pads.
11. The wafer test method of claim 10, wherein a solder mask is applied over the second surface of the core and formed with a plurality of openings for exposing predetermined portions of the conductive traces, allowing the test bumps to be bonded to the exposed portions.
12. The wafer test method of claim 11, wherein the test bumps are electrically connected to the test pads by the corresponding conductive traces and conductive vias.
13. The wafer test method of claim 11, wherein the test bumps are electrically connected and redistributed to the test pads by the corresponding conductive traces and conductive vias.
14. The wafer test method of claim 1, wherein the test bumps are made of gold.